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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/281,358	03/30/1999	ROGER PANICACCI	08305/031001	7144

7590 06/04/2003

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EXAMINER

TRAN, NHAN T

ART UNIT	PAPER NUMBER
2615	10

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/281,358	PANICACCI, ROGER
	Examiner Nhan T. Tran	Art Unit 2615

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 19 March 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-8 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 30 March 1999 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) Interview Summary (PTO-413) Paper No(s). _____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

DETAILED ACTION

Drawings

1. In order to avoid abandonment, the drawing informalities noted in Paper No. 5, mailed on 12/19/2002, must now be corrected. Correction can only be effected in the manner set forth in the above noted paper.

The drawing informalities noted in Paper No. 5 is re-attached in this Office Action.

Response to Arguments

2. Applicant's arguments filed on 3/19/2003 with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 3 & 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Gowda et al (US 6,115,066).

Regarding claim 1, Gowda discloses an active pixel sensor, comprising:

a sensor array of pixels, arranged in logical units (e.g., rows, columns), wherein each pixel comprises a photosensor element (30), an in-pixel buffer element (25, 23), and in-pixel selector element (22) (see Figs. 3 & 4; col. 3, lines 53-57; col. 4, lines 62-64; col. 5, lines 1-3); a plurality analog-to-digital converters (ADC 40₁ – 40_N), formed on the same substrate as said pixel sensor array, and each associated with N logical units (C₁- C_N or 15₁ – 15_N) of the pixel sensor array, each analog-to-digital converter including an ADC portion which receives an analog signal from one of the pixel sensors of a logical unit when the selector element is enabled, and converts said analog signal to a converted digital value, an N storage elements (42₁ – 42_N, 44), each respectively associated with one of plurality of analog to digital converters, and each for storing the converted digital value indicating the output signal; wherein N is at least two (see Figs 3 & 4; col. 3, line 57 – col. 4, line 13). It is noted that each ADC can be tied to multiple column lines 15, meaning N is at least 2.

Regarding claim 2, the logical units are lines of the array including either columns of the array or rows of the array (see Fig. 3).

Regarding claim 3, Gowda discloses that the analog-to-digital converters are associated with at least two adjacent lines of the array (see col. 4, lines 8-13 for each ADC associated with multiple column lines 15).

Regarding claim 8, each pixel is a CMOS pixel (see col. 1, lines 19-22).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al (US 6,115,066) in view of Ando et al (US 4,839,729).

Regarding claim 4, Gowda discloses a readout controller (14), controlling readout of information from the photosensor elements, by controlling said analog-to-digital converters to each convert information of a first line of the array (i.e., one column bus 15), to store the information from the first line of the array in one of said unit storage elements (i.e., register 42) (see Figs. 3 & 4; col. 3, line 57 – col. 4, line 13).

Gowda does not teach each ADC is then read out the second line of the array after the first array, and store the information from the second line of the array in the other of the unit

storage elements, and then to read out the information from all of the unit storage elements in a desired order. However, Ando teaches two separate memories (14, 15) for storing bright signal and dark signal, respectively, read out from two separate logical units (two rows) and then the bright and dark signals are simultaneously derived on the read out lines (LH1 and LH2) from the two separate memories for removing fixed pattern noises (FPN) to obtain a image signal with sufficiently wide dynamic range (see Figs. 2-5; col. 2, lines 15-31).

Therefore, it would have been obvious to one of ordinary skill in the art to implement Gowda with the teaching of Ando for reading out and storing the second line of the array in a separate second storage element and then read out both the information from all of the unit storage element in a desired order for removing fixed pattern noises (FPN) to obtain a image signal with sufficiently wide dynamic range.

5. Claims 5 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al (US 6,115,066) in view of Adiletta (US 6,295,546).

Regarding claim 5, Gowda discloses a method for operating a pixel sensor array, comprising:

obtaining a pixel sensor array of photosensitive elements (20), each having photosensitive element in a pixel, a buffer in the pixel (23, 25) associated with the photosensitive element, and a selector transistor in the pixel (22) which is enabled to allow a signal from the pixel to pass, and disabled to block the signal from passing (see Figs. 3 & 4; col. 3, lines 53-57; col. 4, lines 62-64; col. 5, lines 1-3);

connecting a plurality of said outputs of said selector transistors to one another, to form a plurality of logical units ($15_1 - 15_N$), each logical unit formed by a plurality of said output transistors (30) which are connected to one another (to form one column 15) (see Fig. 3);

receiving, in a plurality of A/D converter units ($40_1 - 40_N$), respective plurality of signals from a respective plurality of first logical units (e.g., signals from pixels 30 in columns 15), and A/D converting said respective plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values information in a respective first storage units (registers $42_1 - 42_N$) as shown in Fig. 3; col. 3, lines 57-67;

receiving, in said plurality of A/D converter units, a respective of signals from a respective plurality of second logical units, adjacent to said first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values (see col. 4, lines 7-13, wherein each A/D converter can be tied to multiple column lines 15), and storing said respective plurality of converted digital values in a respective plurality of second storage units (44) (see col. 6, lines 28-33 for other storage registers within logic block 44);

Gowda does not disclose that information in the A/D converters is read out in a different order than an order in which the information was converted. However, Adiletta teaches a variation of reading out the digital image information from storage units in either little endian or GIB endian format for providing the appropriate output conversion format depending upon the requirements of the coupled peripheral multimedia device (see fig. 43B, col. 63, line 55 – col. 64, line 20).

Art Unit: 2615

Therefore, it would have been obvious to one of ordinary skill in the art to modify Gowda with Adiletta to provide alternative reading out scheme from A/D converters in which the digital image information is read out in either little endian or GIB endian format for providing the appropriate output conversion format depending upon the requirements of the coupled peripheral multimedia device.

Regarding claim 6, the little endian, GIB endian read out order is inherently in a serial order.

Regarding claim 7, Gowda shows that said units are linear units which are one of rows and columns (see Fig. 3). An Official Notice is taken that it is well known in the art for signal processing in which a first order skipping lines between conversions, and second order being a complete order in an imaging system.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

NT.
May 28, 2003



ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600